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UTILITY PATENT APPLICATION TRANSMITTAL

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Attorney Docket No.	LOTFI 22-2
First Inventor or Application Identifier	Ashraf Lotfi, et al.
Title	SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME
Express Mail Label No.	EL176029903US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages 6]
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   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
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Atty. Docket No. Lotfi 22-2 PATENT APPLICATION

SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME

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SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME

TECHNICAL FIELD OF THE INVENTION

The present invention is directed, in general, to semiconductor fabrication and, more specifically, to a silicon carbide metal oxide semiconductor field effect transistor (SiC MOSFET) having high breakdown voltage, a method of manufacturing the same and a semiconductor device incorporating the SiC MOSFET or the method.

BACKGROUND OF THE INVENTION

A power converter is a power processing circuit that converts an input voltage waveform into a specified output voltage waveform. In many applications requiring a stable and well-regulated output, switched-mode power converters are frequently employed for an advantage. Switched-mode power converters generally include an inverter, a transformer having a primary winding coupled to the inverter, an output rectifier coupled to a secondary winding of the transformer, an output filter and a controller. The inverter generally includes a power switch, such as a field-effect

transistor (FET), that converts an input voltage to a switched voltage that is applied across the transformer. The transformer may transform the voltage to another value and the output circuit generates a desired voltage at the output of the converter. The output filter typically includes an inductor and an output capacitor. The output capacitor smooths and filters the output voltage for delivery to a load.

In many power converter applications, the output voltage requirements and therefore the voltage handling requirements of the power switch, are large. In a conventional silicon semiconductor wafer, large voltage handling capability is difficult to achieve in a laterally constructed FET due to the inherently close proximity of the source and drain. This arrangement thereby causes lower than desired values of breakdown voltage for the device. This has often necessitated the use of a power switch called a vertical device metal oxide semiconductor FET (VDMOSFET). The VDMOSFET is constructed such that the drain is positioned on the bottom of the device, and the source is positioned on the top, with the gate vertically interposed between the drain and source. This vertical arrangement allows the VDMOSFET to achieve a larger breakdown voltage, and therefore, allows the VDMOSFET to accommodate a larger operating voltage while using conventional silicon semiconductor wafer technology.

Unfortunately, the VDMOSFET has a greater intrinsic on-resistance, which becomes important when the VDMOSFET is used as a switch, and also possesses a greater intrinsic capacitance. The greater on-resistance and capacitance are due, in part, to the increased separation of the source and drain and the added layers needed to obtain the larger breakdown and operating voltage capability. The greater on-resistance of the VDMOSFET increases the losses contributed by the VDMOSFET and may therefore reduce an overall efficiency of a power converter employing the VDMOSFET. Additionally, the added capacitance decreases switching speed and therefore may increase switching losses as well.

Another problem arises from the general trend of such electronic devices toward ever smaller device sizes and ever greater packing density. As the VDMOSFET's size continues to shrink and device packing density increases, the junction field effect transistor resistance of the vertical region between the two adjacent P wells also increase, thereby inhibiting the performance of the device even further. Thus, the VDMOSFET's use in such power converters may be substantially limited in the near future due to these physical limitations.

Accordingly, what is needed in the art is a MOSFET that provides an advantageous breakdown voltage characteristic while exhibiting a low on-resistance as a switch.

SUMMARY OF THE INVENTION

To address the above-discussed deficiencies of the prior art, the present invention provides a lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over or within a substrate of a semiconductor wafer, a method of manufacturing the same and a semiconductor device incorporating the MOSFET or the method. In one embodiment, the MOSFET includes a silicon carbide layer that is located over or within, and preferably on, the substrate having a gate, which is formed on the silicon carbide layer. Source and drain regions are located in the silicon carbide layer and are laterally offset from the gate. In a preferred embodiment, the silicon carbide has a breakdown field greater than a breakdown field of silicon. For example, in one particularly advantageous embodiment, the breakdown voltage of the silicon carbide heavily doped p-n junction is at least about 10 volts.

The present invention therefore introduces the broad concept of employing silicon carbide in a lateral MOSFET device to increase a breakdown voltage of the MOSFET. The breakdown voltage is a critical parameter affecting a range of applications for the MOSFET device. The breakdown voltage is of particular importance in MOSFET devices that are employed as switches in power related applications, such as power converters. The lateral MOSFET device

offers additional advantages, particularly in power application embodiments, since its on-resistance as a switch is inherently lower than vertically structured devices. The inherently lower on-resistance raises the efficiency of power converters and other switching devices employing the lateral MOSFET. Additionally, the ability to integrate silicon carbide lateral MOSFET devices and complementary metal oxide semiconductor (CMOS) devices onto the same semiconductor wafer allows power supplies to be located in close proximity to their load circuits.

The source and drain regions of the MOSFET are preferably doped with an N-type dopant and are preferably formed in a tub doped with a P-type dopant.

In another embodiment, the MOSFET further includes a buried oxide layer. The buried oxide layer may be formed in the substrate. However, in one advantageous embodiment, it is formed in the substrate. The gate and substrate may be comprised of conventional materials, such as poly-silicon and silicon, respectfully. In those embodiments where the silicon carbide is formed on a silicon substrate, a 3C silicon carbide structure is formed. In yet another embodiment, the MOSFET is formed on a semiconductor wafer that includes a CMOS device, which, in certain embodiments, may form a drive controller for a power converter.

The MOSFET device as provided by the present invention may have various uses. One particular useful application is where the MOSFET is a power switch employed in a power train of a power converter.

Another aspect of the present invention provides a method of forming a lateral MOSFET over or within a substrate of a semiconductor wafer. In one embodiment, the method comprises forming a silicon carbide layer over the substrate, forming a gate on the silicon carbide layer, and forming source and drain regions in the silicon carbide layer laterally offset from the gate. The method may further include annealing the source and drain regions at about 1200° C.

As was the case with the device, the method may also comprise forming a buried oxide layer in the substrate. However, in preferred embodiments, the buried oxide layer is formed in the substrate. Moreover, forming source and drain regions may comprise implanting an N-type dopant into the silicon carbide layer, which may be doped with a P-type dopant.

In a preferred embodiment, the silicon carbide layer is formed on the substrate, which may be a silicon substrate. In such embodiments, a 3C silicon carbide layer may be formed.

In another embodiment, the method includes configuring the MOSFET as a power switch and integrating the MOSFET into a power converter.

In another aspect, the present invention provides a power converter that includes an isolation transformer, a primary side power switch coupled to a primary winding of the isolation transformer and a secondary side power switch coupled to a secondary winding of the isolation transformer. It should be understood that any switch employed in the power converter may include the a lateral MOSFET as provided by the present invention. The power converter further includes a drive circuit coupled to the secondary side power switch. The drive circuit preferably includes a CMOS device formed on a silicon substrate and has an operating voltage that is lower than the breakdown voltage of the MOSFET. An output inductor coupled to the secondary side power switch and an output capacitor coupled to the output inductor also form a part of the power converter.

The MOSFET incorporated into the power converter preferably includes a silicon carbide layer located over or within the substrate, a gate formed on the silicon carbide layer, and source and drain regions located in the silicon carbide layer and laterally offset from the gate. In such embodiments, the operating

voltage may range from about 3 volts to 5 volts while the breakdown voltage may range from about 10 volts to 30 volts.

As with previous embodiments, the MOSFET may further include a buried oxide layer, which may be located in the substrate. Additionally, the source and drain regions may be doped with an N-type dopant, while the tub in which the source and drain regions are formed may be doped with a P-type dopant. In those embodiments where the silicon is formed on a silicon substrate, a 3C silicon carbide is formed.

In yet another aspect, the present invention provides a method of forming a power converter. In a preferred embodiment, the method includes forming an isolation transformer, forming a primary side power switch coupled to a primary winding of the isolation transformer and forming a secondary side power switch coupled to a secondary winding of the isolation transformer. It should be understood that any switch employed in the power converter may be a lateral MOSFET as provided by the present invention. The method further comprises forming a drive circuit coupled to the secondary side power switch, including a CMOS device formed on a silicon substrate and having an operating voltage, wherein the MOSFET has a breakdown voltage higher than the operating voltage of the CMOS device, forming an output inductor coupled to the secondary side

power switch, and forming an output capacitor coupled to the output inductor, the secondary side power switch.

Another aspect of this particular method includes annealing the source and drain regions at about 1200°C and may also include forming an oxide layer over the silicon carbide layer employing chemical vapor deposition. Preferably, the oxide layer is annealed at about 950°C.

The foregoing has outlined, rather broadly, preferred and alternative features of the present invention so that those skilled in the art may better understand the detailed description of the invention that follows. Additional features of the invention will be described hereinafter that form the subject of the claims of the invention. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiment as a basis for designing or modifying other structures for carrying out the same purposes of the present invention. Those skilled in the art should also realize that such equivalent constructions do not depart from the spirit and scope of the invention in its broadest form.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a semiconductor wafer including an embodiment of a lateral MOSFET constructed in accordance with the principles of the present invention;

FIGURE 2A illustrates a sectional view of a MOSFET covered by the present invention an intermediate stage of manufacture;

FIGURE 2B illustrates a sectional view of the MOSFET of FIGURE 2A at a subsequent intermediate stage of manufacture;

FIGURE 2C illustrates a sectional view of the MOSFET of FIGURE 2B at a subsequent intermediate stage of manufacture;

FIGURE 2D illustrates a sectional view of the MOSFET of FIGURE 2C at a subsequent intermediate stage of manufacture;

FIGURE 2E illustrates a sectional view of another embodiment of the MOSFET as covered by the present invention;

FIGURE 2F illustrates a sectional view of another embodiment of the MOSFET as covered by the present invention;

FIGURE 3A illustrates an embodiment of a semiconductor wafer showing an integrated structure employing a silicon carbide lateral

MOSFET and CMOS devices constructed in accordance with the principles of the present invention;

FIGURE 3B illustrates another embodiment of a semiconductor wafer showing an integrated structure employing a silicon carbide lateral MOSFET and CMOS devices constructed in accordance with the principles of the present invention and having an insulator incorporated therein; and

FIGURE 4 illustrates a schematic diagram of a power converter into which the previously discussed MOSFET and CMOS devices may be incorporated.

DETAILED DESCRIPTION

Referring initially to FIGURE 1, illustrated is a semiconductor wafer 100 including an embodiment of a lateral MOSFET 107 constructed in accordance with the principles of the present invention. The semiconductor wafer 100 includes a substrate 105 and the lateral MOSFET 107, which is formed over the substrate 105. In the present embodiment, the lateral MOSFET 107 includes a silicon carbide layer 110 located over the substrate 105. The lateral MOSFET has a gate 121. The gate 121 is formed having a gate layer 120 on a gate oxide layer 115, which is formed on the silicon carbide layer 110. Source and drain regions 125, 130 respectively, are conventionally formed in the silicon carbide layer 110. The source and drain regions 125, 130 are laterally offset from the gate as shown and are in contact with the gate 121.

In the illustrated embodiment, the substrate 105 and the silicon carbide layer 110 are doped with a P-type dopant, such as aluminum or boron. The gate structure 121 is preferably of conventional design and formed by conventional processes and may include a poly-silicon gate formed silicon dioxide gate oxide. The source and drain regions 125, 130 are conventionally implanted in the silicon carbide layer 110 as shown. The source and drain regions 125, 130 are preferably doped with an N-type dopant, such

as nitrogen, arsenic or phosphorous. Of course, other materials may be used as the N-type dopants or the P-type dopants.

The present invention, therefore, employs silicon carbide in the lateral MOSFET 107 to increase the breakdown voltage of the lateral MOSFET 107. The breakdown voltage of the lateral MOSFET 107 is typically in the range of about 10 volts to 30 volts or higher as previously discussed. This range of breakdown voltage is determined by the doping parameters of the silicon carbide layer 110 and the size of the gate geometry being applied. The breakdown voltage of the lateral MOSFET 107 is typically chosen to be substantially above an operating voltage determined by other conventionally-formed devices, such as a CMOS that may also be employed in the semiconductor wafer 100.

The breakdown voltage is a critical parameter affecting a range of applications for the lateral MOSFET 107. An application of particular importance encompasses an embodiment of the present invention wherein the lateral MOSFET 107 is employed as a switch in a power related application, such as a power converter. The lateral MOSFET 107 offers an additional advantage along with higher breakdown voltage. The total on-resistance of the MOSFET 107, when used as a switch, is inherently lower than the total resistance associated with vertically structured devices or lateral devices on silicon with the same breakdown voltage. The total on-resistance

of the MOSFET 107 is typically composed of just a channel resistance (often designated R_{CH}) between the source 125 and the drain 130. An inherently lower on-resistance raises the efficiency of the lateral MOSFET 107 as a power switch compared to a typical vertically structured device and in other switching applications, as well.

In an alternate embodiment to be illustrated and discussed, the ability to integrate the lateral MOSFET 107 and CMOS devices into the semiconductor wafer 100 allows power supplies to be located in close proximity to their load circuits. This capability is extremely valuable, since it allows the diverse power requirements for groups of CMOS devices having different operating voltages to be accommodated on the semiconductor wafer 100. Separate power supplies for groups of CMOS devices having the same operating voltage allows the groups to be better isolated electrically thereby reducing and containing inherent noise interference on the semiconductor wafer 100.

Turning now to FIGUREs 2A through 2D, illustrated are sectional views of a MOSFET 200 covered by the present invention at various stages of manufacture. In FIGURE 2A, illustrated is a substrate 205 and a silicon carbide layer 210. The silicon carbide layer 210 is formed on the substrate 205 by growing a cubic crystalline silicon carbide in the presence of a P-type dopant,

such as aluminum or boron, thereby forming a tub for further implantation. In a preferred embodiment, the deposition of the silicon carbide layer 210 may be carried out in a quartz reaction tube at a temperature of about 900°C with trimethoisilane as a source gas or using other conventional methods. As previously mentioned, the silicon carbide layer 110 provides distinct advantages over prior art materials, such as silicon, in that it provides a much higher breakdown field. Moreover, due to its configuration, the MOSFET is capable of behaving like an NMOS device, but is capable of holding off a much higher voltage than a typical NMOS device. These aspects allow the MOSFET to be easily integrated into a CMOS device with applications toward various technologies requiring high breakdown voltages, such as power converters.

Following the formation of the silicon carbide layer 210, a photoresist layer 215 is then conventionally deposited on the silicon carbide layer 210 and patterned as show in FIGURE 2B. FIGURE 2C illustrates the MOSFET 200 wherein an unwanted portion of the silicon carbide layer 210 has been conventionally etched away and the photoresist layer 215 has been removed, thereby defining the area for the silicon carbide lateral MOSFET.

FIGURE 2D illustrates the MOSFET 200 wherein a source 225 and a drain 230 are formed by implanting an N-type dopant into the

silicon carbide layer 210. The N-type dopant is preferably phosphorous. Of course, nitrogen or another N-type dopant may be used as appropriate. The source 225 and the drain 230 regions are then annealed at about 1200°C to activate the dopant. A silicon carbide base is thus provided on which the lateral MOSFET 107 that is suitable for use in devices requiring high breakdown voltages is subsequently formed.

FIGURE 2E illustrates yet another embodiment, in which the MOSFET device 200 may be formed over a substrate having an insulator layer 240 formed therein, which is typically known as a buried oxide layer or a silicon-on-insulator. The insulator layer 240 is conventionally formed prior to the formation of the silicon carbide layer 210. The insulator layer 240 provides the advantage of reducing the overall parasitic capacitance that exists in integrated circuit devices.

FIGURE 2F illustrates still another embodiment, in which the MOSFET device 200 may be formed within a substrate 205 having an insulator layer 240 formed therein, which was discussed in FIGURE 2E. In such embodiments, a silicon trench 209 is conventionally formed in the substrate 205 prior to the formation of the silicon carbide layer 210. The silicon carbide layer 210 is then deposited in the silicon trench 209. Of course, another embodiment of the present invention may form the silicon trench 209 and the silicon

carbide layer 210 within a substrate that does not have the insulator layer 240. Following the formation of the silicon carbide layer 210, a gate is formed on the silicon carbide layer 210 in the manner discussed herein for other embodiments.

Turning now to FIGURE 3A, illustrated is an embodiment of a semiconductor wafer showing an integrated structure employing a silicon carbide lateral MOSFET 307 and silicon CMOS devices 334, 345 constructed in accordance with the principles of the present invention. In this particular embodiment, the semiconductor wafer 300 includes a P-type doped silicon substrate 305 having first and second CMOS devices 334, 345 and a silicon carbide lateral MOSFET 307 as provided by the present invention formed thereon. The first CMOS device 334 is a PMOS transistor, and the second CMOS device 345 is an NMOS transistor, both of which are of conventional design and formed by conventional processes. As such, the first CMOS device 334 includes an N-doped tub region 335, a gate 338 and P-doped source and drain regions 336, 339 in contact with the gate 338. The second CMOS device 345 includes a P-doped tub region 340, a gate 343 and N-doped source and drain regions 341, 344 in contact with the gate 343. In this particular embodiment, the silicon carbide lateral MOSFET 307, includes a silicon carbide layer 310 containing a P-type dopant, a gate 321 and N-doped source and drain regions 325, 330 in contact with the gate 321. The gates 338, 343

and 321 are poly-silicon formed over a gate oxide such as silicon dioxide.

In this particular configuration, the lateral MOSFET 307 may have a breakdown voltage of about 10 volts to 30 volts, or higher, that is substantially higher than the operating voltage of about 3 volts to 5 volts for the first and second CMOS devices 334, 345. In the illustrated embodiment, the lateral MOSFET 307 may be employed as a power switch in a power converter. This aspect of the present invention is later discussed in more detail.

A method for constructing the semiconductor wafer 300 incorporates the figures as depicted in FIGURES 2A through 2D to construct the silicon carbide lateral MOSFET 307, up to the silicon carbide layer gate level, which is later defined. Once the silicon carbide layer 310 has been constructed, the first and second CMOS devices 334, 345 are then conventionally constructed on the substrate 305 up to the ohmic contacts, which are later defined. Following the formation of the CMOS devices 334, 345, a plasma enhanced tetraethyl orthosilciate oxide (PETEOS) layer 346 is conventionally deposited over the CMOS devices 334, 345 to isolate them from the MOSFET 307 gate oxide and gate formation processes. A MOSFET 307 gate oxide layer is first deposited followed by a 950°C re-ox anneal. Then, a MOSFET 307 gate layer, such as polysilicon is then deposited over the gate oxide layer. These

layers are then conventionally patterned and etched to form a gate oxide layer 315 and a gate 320 as shown in FIGURE 3A. Metal ohmic contacts, which are not shown, are then formed for the lateral MOSFET 307 and annealed in argon at about 900°C, which are followed by the formation of CMOS device ohmic contacts that are annealed at about 450°C. FIGURE 3B simply illustrates how the previously discussed insulator layer 350 might appear in one embodiment where the MOSFET device 307 is integrated into a CMOS circuit.

Turning now to FIGURE 4, there is illustrated a schematic diagram of a power converter 400 into which the previously discussed MOSFET and CMOS devices may be incorporated. In the illustrated embodiment, the power converter 400 includes an isolation transformer 410, a primary side power switch 415 coupled to a primary winding 420 of the isolation transformer 410. The power converter 400 further includes a secondary side power switch 425 that is coupled to a secondary winding 430 of the isolation transformer 410. It should be understood that any of the switches employed in the power converter 400 may include the MOSFET covered by the present invention, which has been described above.

The power converter 400, in a preferred embodiment, further includes a primary side control drive circuit 435 coupled to the primary side power switch 415 and a secondary drive circuit 440 coupled to the secondary side power switch 425. In a preferred

embodiment, either or both of the drive circuits 435, 440 may include a CMOS device, which is preferably formed on the same silicon substrate as the MOSFET. The CMOS device preferably has an operating voltage that is lower than a breakdown voltage of the MOSFET. As discussed above, the breakdown voltage of the MOSFET is preferably substantially higher than the operating voltage of the CMOS device. The power converter 400 further includes an output inductor 445 coupled to the secondary side power switch 425 and an output capacitor 450 coupled to the output inductor 440.

Those skilled in the art should understand that the previously described embodiment of the power converter is submitted for illustrative purposes only and other power converter topologies such as half bridge, full bridge, flyback, and boost converter topologies employing discrete or integrated magnetics are well within the broad scope of the present invention. Additionally, exemplary embodiments of the present invention have been illustrated with reference to specific electronic components. Those skilled in the art are aware, however, that components may be substituted (not necessarily with components of the same type) to create desired conditions or accomplish desired results. For instance, multiple components may be substituted for a single component and vice-versa.

Although the present invention has been described in detail, those skilled in the art should understand that they can make various changes, substitutions and alterations herein without departing from the spirit and scope of the invention in its broadest form.

WHAT IS CLAIMED IS:

1. A lateral metal-oxide semiconductor field effect transistor (MOSFET), comprising:

a silicon carbide layer located over or within a substrate of a semiconductor wafer, a gate formed on the silicon carbide layer; and

source and drain regions located in the silicon carbide layer and laterally offset from the gate.

2. The MOSFET as recited in Claim 1 wherein the silicon carbide layer has a breakdown voltage greater than a breakdown voltage of silicon.

3. The MOSFET as recited in Claim 2 wherein the silicon carbide layer has a breakdown voltage of at least about 10 volts.

4. The MOSFET as recited in Claim 1 wherein the source and drain regions are doped with an N-type dopant.

5. The MOSFET as recited in Claim 1 wherein the source and drain regions are formed in a tub doped with a P-type dopant.

6. The MOSFET as recited in Claim 1 further comprising a buried oxide layer formed in the substrate.

7. The MOSFET as recited in Claim 1 wherein the silicon carbide layer is formed on the substrate.

8. The MOSFET as recited in Claim 7 wherein the substrate comprises silicon and the silicon carbide is a 3C silicon carbide.

9. The MOSFET as recited in Claim 1 wherein the MOSFET is located on a semiconductor wafer that includes a CMOS device.

10. The MOSFET as recited in Claim 1 wherein the MOSFET is a power switch employed in a power train of a power converter.

11. A method of forming a lateral metal-oxide semiconductor field effect transistor (MOSFET) over or within a substrate of a semiconductor wafer, comprising:

forming a silicon carbide layer over the substrate;

forming a gate on the silicon carbide layer; and

forming source and drain regions in the silicon carbide layer laterally offset from the gate.

12. The method as recited in Claim 11 further comprising annealing the source and drain regions at about 1200° C.

13. The method as recited in Claim 11 further comprising forming a buried oxide layer.

14. The method as recited in Claim 13 wherein forming a buried oxide layer includes forming a buried oxide layer in the substrate.

15. The method as recited in Claim 11 wherein forming source and drain regions comprises implanting an N-type dopant into the silicon carbide layer.

16. The method as recited in Claim 11 wherein forming source and drain regions comprises forming the source and drain regions in a tub doped with a P-type dopant.

17. The method as recited in Claim 11 wherein forming a silicon carbide layer includes forming the silicon carbide layer on the substrate.

18. The method as recited in Claim 17 wherein forming a silicon carbide layer on the substrate includes forming a 3C silicon carbide layer on a silicon substrate.

19. The method as recited in Claim 11 further comprising configuring the MOSFET as a power switch and integrating the MOSFET into a power converter.

20. The method as recited in Claim 11 wherein forming a MOSFET includes forming the MOSFET on a semiconductor wafer that includes a CMOS device.

21. A power converter, comprising:

an isolation transformer;

a primary side power switch coupled to a primary winding of the isolation transformer, and a secondary side power switch coupled to a secondary winding of the isolation transformer, wherein at least one of the primary side power switch or the secondary side power switch is a lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over or within a substrate of a silicon wafer;

a drive circuit coupled to the secondary side power switch and including a complementary metal oxide semiconductor (CMOS) device formed on a silicon substrate and having an operating voltage, the MOSFET having a breakdown voltage higher than the operating voltage of the CMOS device;

an output inductor coupled to the secondary side power switch; and

an output capacitor coupled to the output inductor.

22. The power converter as recited in Claim 21 wherein the MOSFET includes:

a silicon carbide layer located over or within the substrate, a gate formed on the silicon carbide layer, and

source and drain regions located in the silicon carbide layer and laterally offset from the gate.

23. The power converter as recited in Claim 21 wherein the operating voltage ranges from about 3 volts to 5 volts and the breakdown voltage ranges from about 10 volts to 30 volts.

24. The power converter as recited in Claim 21 further comprising a buried oxide layer.

25. The power converter as recited in Claim 24 wherein the buried oxide layer is located in the substrate.

26. The power converter as recited in Claim 21 wherein the source and drain regions are doped with an N-type dopant.

27. The power converter as recited in Claim 21 wherein the silicon carbide is 3C silicon carbide.

28. The power converter as recited in Claim 21 wherein the source and drain regions are formed in a tub doped with a P-type dopant.

29. The power converter as recited in Claim 21 wherein the silicon carbide layer is formed on the silicon substrate.

30. The power converter as recited in Claim 21 wherein the gate comprises polysilicon and the substrate comprises silicon doped with a P-type dopant.

31. A method of forming a power converter, comprising:

forming an isolation transformer;

forming a primary side power switch coupled to a primary winding of the isolation transformer;

forming a secondary side power switch coupled to a secondary winding of the isolation transformer, at least one of the primary side power switch and the secondary side power switch being a lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over or within a substrate of a silicon wafer;

forming a drive circuit coupled to the secondary side power switch and including a complementary metal oxide semiconductor (CMOS) device formed on a silicon substrate and having an operating voltage, the MOSFET having a breakdown voltage higher than the operating voltage of the CMOS device;

forming an output inductor coupled to the secondary side power switch; and

forming an output capacitor coupled to the output inductor, the secondary side power switch.

32. The method as recited in Claim 31 wherein forming a MOSFET includes:

forming a silicon carbide layer over or within the substrate;

forming a gate on the silicon carbide layer; and

forming source and drain regions in the silicon carbide layer and in contact with the gate.

33. The method as recited in Claim 31 further comprising annealing the source and drain regions at about 1200° C.

34. The method as recited in Claim 31 further comprising forming a buried oxide layer.

35. The method as recited in Claim 34 wherein forming a buried oxide layer includes forming a buried oxide layer in the substrate.

36. The method as recited in Claim 31 wherein forming the source and drain regions comprises implanting an N-type dopant into the silicon carbide layer.

37. The method as recited in Claim 31 wherein forming the source and drain regions comprises forming the source and drain regions in a tub doped with a P-type dopant.

38. The method as recited in Claim 31 wherein forming a silicon carbide layer includes forming the silicon carbide layer on the substrate.

39. The method as recited in Claim 31 wherein forming the silicon carbide layer on the substrate includes forming the silicon carbide layer on a silicon substrate.

40. The method as recited in Claim 31 further comprising forming an oxide layer over the silicon carbide layer employing chemical vapor deposition.

41. The method as recited in Claim 40 further comprising annealing the oxide layer at about 950° C.

42. The method as recited in Claim 31 wherein forming a silicon carbide layer includes forming a 3C silicon carbide layer.

43. The method as recited in Claim 31 wherein forming a CMOS device includes forming the CMOS device to have an operating voltage ranging from about 3 volts to about 5 volts and forming a MOSFET includes forming a MOSFET having a breakdown voltage ranging from about 10 volts to about 30 volts.

SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME

ABSTRACT OF THE DISCLOSURE

A lateral metal-oxide semiconductor field effect transistor (MOSFET) formed over a substrate of a semiconductor wafer, a method of manufacturing the same and a semiconductor device incorporating the MOSFET or the method. In one embodiment, the MOSFET includes a silicon carbide layer located over or withing the substrate, a gate formed on the silicon carbide layer. The MOSFET further includes source and drain regions located in the silicon carbide layer and in contact with the gate, the silicon carbide layer increasing a breakdown voltage of the MOSFET.

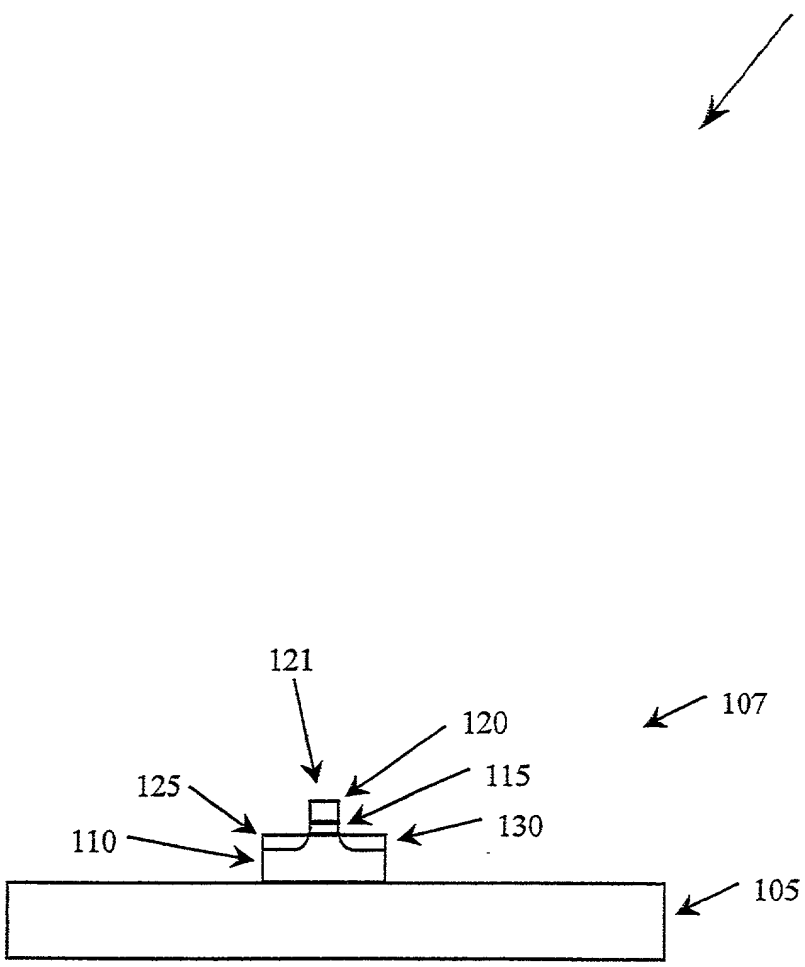


FIGURE 1

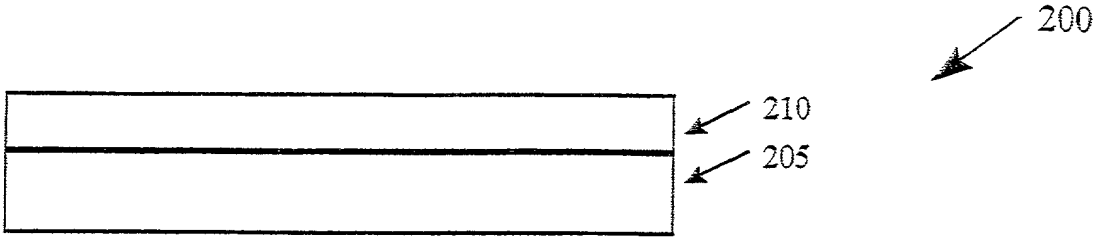


FIGURE 2A

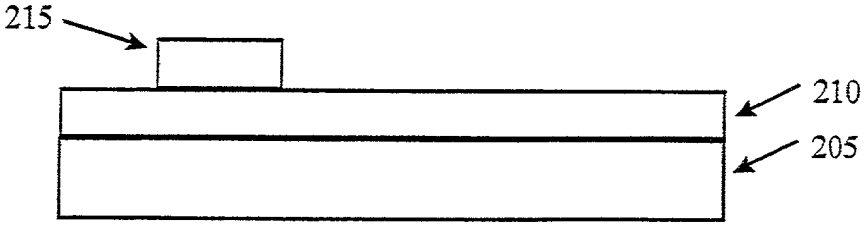


FIGURE 2B

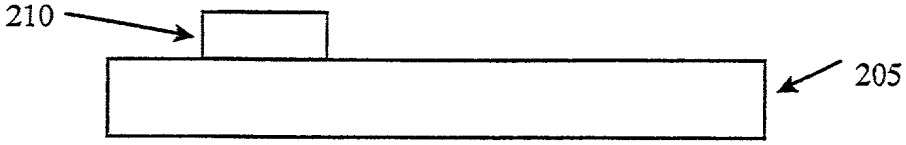


FIGURE 2C

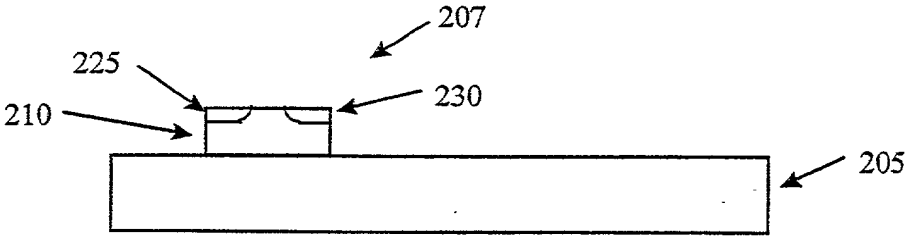


FIGURE 2D

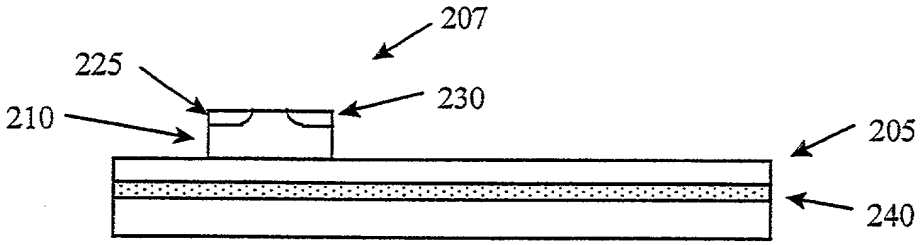


FIGURE 2E

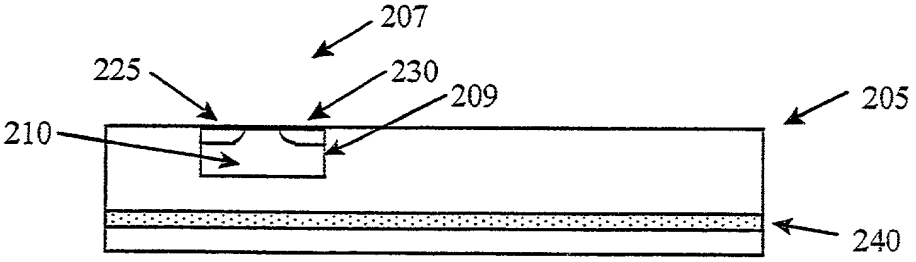
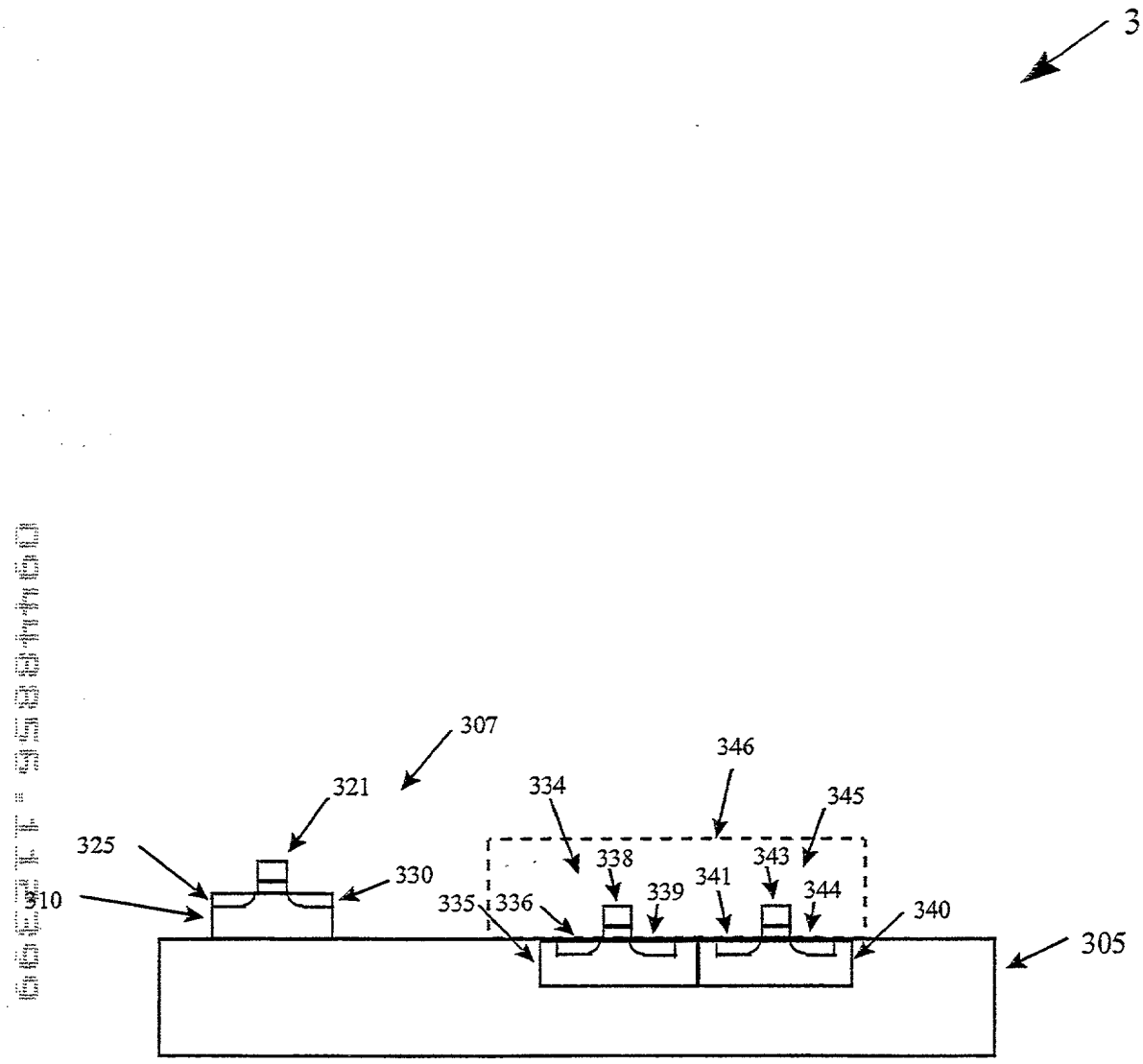


FIGURE 2F


300
307
321
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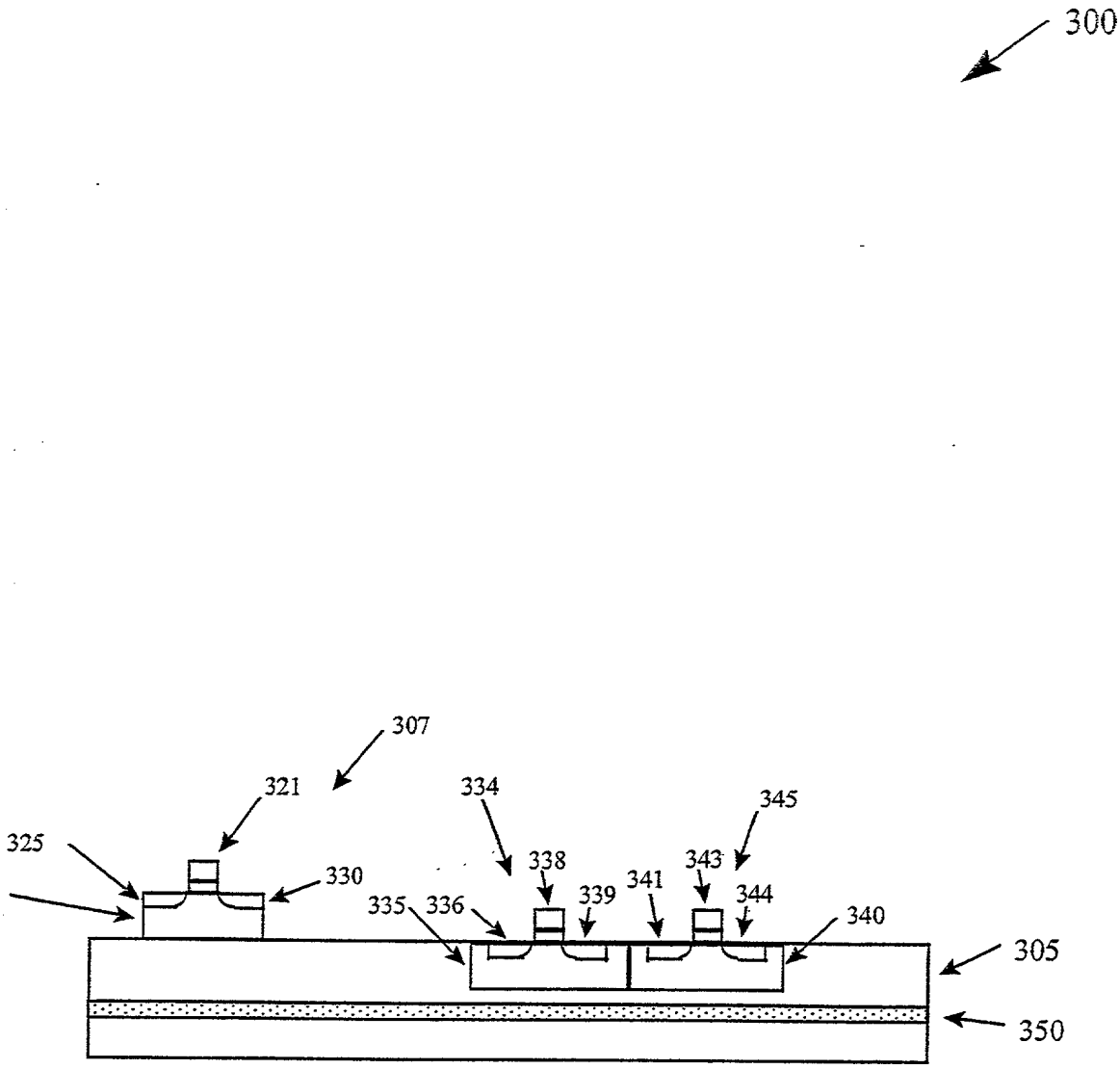
340
305

FIGURE 3A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350

FIGURE 3B

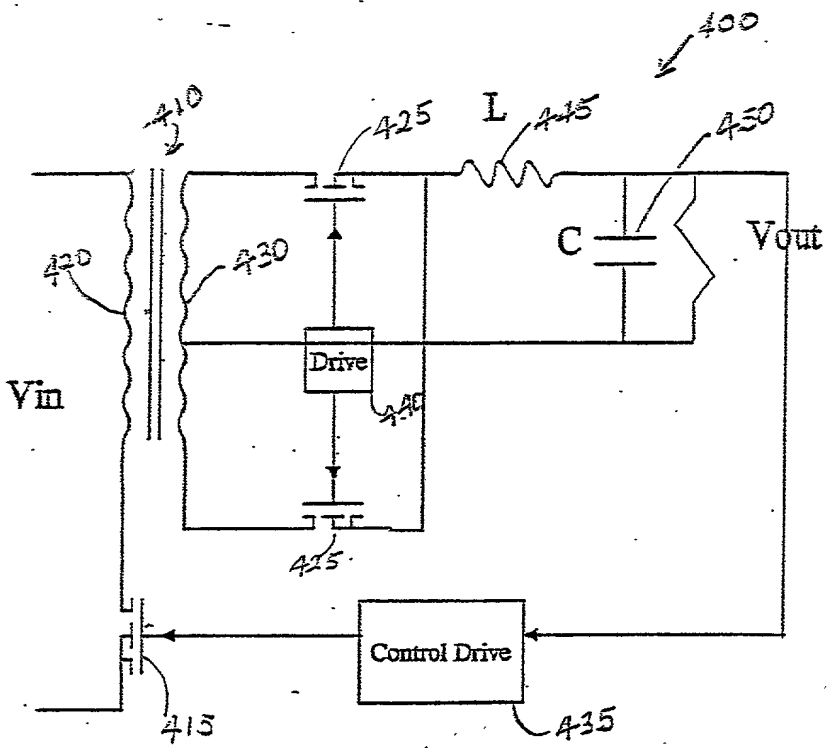
400
410
425
L
445
430
420
430
C
Vout
Vin
Drive
440
425
Control Drive
415
435

FIGURE 4

ATTORNEY DOCKET NO.: LOTFI 22-2 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Delcaration and Power of Attorney

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled "SiC NMOSFET FOR USE AS A POWER SWITCH AND A METHOD OF MANUFACTURING THE SAME," the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment, if any, specifically referred to in this oath or declaration.

I acknowledge the duty to disclose to all information known to me which is material to the patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

NUMBER	COUNTRY	DATE FILED	PRIORITY CLAIMED
None			

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

US/PCT Serial Num	Date Filed	Status
None		

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) with full power of substitution and revocation, to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected therewith:

Lester H. Birnbaum	(Reg. No. 25,830)
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Kenneth M. Brown	(Reg. No. 37,590)
Craig J. Cox	(Reg. No. 39,643)
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Guy Eriksen	(Reg. No. 41,736)
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Ronald D. Slusky	(Reg. No. 26,585)
David L. Smith	(Reg. No. 30,592)
Patricia A. Verlangieri	(Reg. No. 42,201)
John P. Veschi	(Reg. No. 39,058)
David Volejnicek	(Reg. No. 29,355)
Charles L. Warren	(Reg. No. 27,407)
Jeffrey M. Weinick	(Reg. No. 36,304)
Eli Weiss	(Reg. No. 17,765)

I hereby appoint the attorney(s) on ATTACHMENT A as associate attorney(s) in the aforementioned application, with full power solely to prosecute said application, to make alterations and amendments therein, to receive the patent, and to transact all business in the Patent and Trademark Office connected with the prosecution of said application. No other powers are granted to such associate attorney(s) and such associate attorney(s) are specifically denied any power of substitution or revocation.

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Inventor's signature: ____________	Date: 11-22-99
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Full name of second inventor: Jian Tan

Inventor's signature: Jian Tan Date: 11/15/99

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Atty. Docket No.: LOTFI 22-2